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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,423	06/30/2003	Zurab Khasidashvili	INTEL-0022	8079

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,423	KHASIDASHVILI ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/30/03, 11/14/03, 11/17/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *9-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Application filed on 6/30/2003, IDS, drawings and Oath and Declaration filed on 11/14/2003, and IDS transmittal letter filed on 11/17/2003. Claims 1-24 are pending.

Drawings

2. The drawings were received on 11/14/2003. These drawings are approved by the Examiner.

Information Disclosure Statement

3. The IDS submitted on 11/14/2003 was filed without the attorney's signature in the transmittal letter. Such signature as provided on the supplemental transmittal filed on 11/17/2003 is acknowledged. Accordingly, the IDS filed on 11/14/2003 has been considered, as given in the attached IDS.

4. The prior art citation "Gabriel P. Bischoff, Karl S. Brace...." in the IDS filed on 11/14/2003, has been corrected as it properly appeared in the IEEE publication, to:

Bischoff et al., "Formal Implementation Verification of the Bus Interface Unit for the Alpha 21264 Microprocessor", Proceedings of the 1997 IEEE International Conference on Computer Design: VLSI Computers and Processors, 12 October 1997, pp. 16-24.

This prior art has been considered as shown in the attached IDS filed on 11/14/2003.

Claim Objections

5. **Claims 4-24** are objected to because of the following informalities:

As per **claim 4**, "claim 1" (line 1) should be --claim 3-- to provide for proper antecedent basis for "the mathematical expression" (line 2).

As per **claim 5**, "expression" (line 2) should be --representation-- for proper antecedent basis;

--, wherein said BED is defined as $\sum\pi\, a^*_{j[ej1,ej2,...,ejk]}$, wherein $a^*_{j[ej1,ej2,...,ejk]}$ are primitive Retimed Normal Forms (RNFs) and correspond to a value of a_j at a last time signal e_{j1} became high, before signal e_{j2} became high, ..., before e_{jk} became high, wherein j and k are integers-- should be inserted after "(BED)" (line 2) to clearly define the Binary Expression Diagram since applicant's specification does not clearly define this expression (see Applicant's specification, pages 5-6).

As per **claim 6**, --, wherein said BED is defined as $\sum\pi\, a^*_{j[ej1,ej2,...,ejk]}$, wherein $a^*_{j[ej1,ej2,...,ejk]}$ are primitive Retimed Normal Forms (RNFs) and correspond to a value of a_j at a last time signal e_{j1} became high, before signal e_{j2} became high, ..., before e_{jk} became high, wherein j and k are integers-- should be inserted after "(BED)" (line 3) to clearly define the Binary Expression Diagram since applicant's specification does not clearly define this expression (see Applicant's specification, pages 5-6).

As per **claim 7**, "the TBEDs" should be --TBEDs-- for proper antecedent basis since only the singular form "TBED" were previously recited.

As per **claims 7-8**, the claims are also objected to for incorporating the above error into the claims by claim dependency.

As per **claim 9**, "the latches" (line 2) should be --latches-- for proper antecedent basis; "the latch functions" (line 3) should be --latch functions-- for proper antecedent basis; "a binary format" (lines 4-5) should be --the binary format-- to clearly identify that it is the "binary format" recited in line 3.

As per **claims 10,23**, --, wherein said BED is defined as $\sum\pi\, a^*_{j[ej1,ej2,\ldots,ejk]}$, wherein $a^*_{j[ej1,ej2,\ldots,ejk]}$ are primitive Retimed Normal Forms (RNFs) and correspond to a value of a_j at a last time signal e_{j1} became high, before signal e_{j2} became high, ..., before e_{jk} became high, wherein j and k are integers-- should be inserted after "(BED)" (line 2) to clearly define the Binary Expression Diagram since applicant's specification does not clearly define this expression (see Applicant's specification, pages 5-6).

As per **claim 12**, "the TBEDs" (line 1) should be --TBEDs-- for proper antecedent basis since only the singular form "TBED" was previously recited; --,-- (coma) should be inserted after "equivalent" (line 2) for proper grammar and for greater clarification.

As per **claim 16**, "circuit" (line 1) should be deleted for proper antecedent basis.

As per **claim 19**, "the user" (line 2) should be --a user-- for proper antecedent basis.

As per **claims 10-19**, the claims are also objected to for incorporating the above errors into the respective claims by claims dependency.

As per **claim 20**, "a binary format" (line 4) should be --the binary format-- to clearly identify that it is the same as the "binary format" recited in line 3.

As per **claim 22**, "the latches" (line 2) should be --latches-- for proper antecedent basis; "the latch functions" (line 3) should be --latch functions-- for proper antecedent basis; "a binary format" (lines 4-5) should be --the binary format-- to clearly identify that it is the same "binary format" recited in line 3.

As per **claims 21,23-24**, the claims are also objected to for incorporating the above error into the respective claims by claim dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 1-8** are rejected under 35 U.S.C. 102(b) as being anticipated by **Bischoff et al.** ("Formal Implementation Verification of the Bus Interface Unit for the Alpha 21264 Microprocessor", Proceedings of the 1997 IEEE International Conference on Computer Design: VLSI Computers and Processors, 12 October 1997, pp. 16-24).

As per **claims 1-5**, the formal equivalence verification is discussed in the abstract (page 16), wherein the use of the Ternary Binary Decision Diagram (TBDD) as represented by the BDDs as described in section 5 (page 18) the Boolean representation which is a mathematical expression of the component of the circuit including sequential circuit (see page 16, last paragraph--i.e., latches and combinational

logic), wherein such BDDs are characterized with the output of the circuit as a combinational function of a set of input values as further described on page 19, col. 1; wherein since Applicant's specification does not clearly define what BED (Binary Expression Diagram) is, the use of the expression out=in [!clk, clk] as described on page 19, col. 1, are also equivalent to the exemplary BED expression as discussed in Applicant's specification, pages 5-6.

As per **claim 6**, the formal equivalence verification is discussed in the abstract (page 16), wherein the computation of the Timed Binary Expression Diagram (TBED) is illustrated in Fig. 3, as part of the TTBDD (see page 19) based on the BDD since Applicant's specification does not clearly define what BED (Binary Expression Diagram) is, the use of the expression out=in [!clk, clk] as described on page 19, col. 1, are also equivalent to the exemplary BED expression as discussed in Applicant's specification, pages 5-6, and the Timed Ternary BDD would accordingly corresponds to the TBED, as claimed; wherein the applying to the SAT solver or BDD tool to establish equivalent is part of the applying to the BOVE (page 19, col. 1, paragraph 2; sections 4 and 5).

As per **claim 7**, all of the elements of claim 6, from which the claim depends, are discussed in the rejection of claim 6 above, wherein the further comparison of the TBEDs (i.e., TBDDs) of a specification circuit (i.e., schematic) and an implementation circuit (i.e., RTL) is also described in section 5, page 18.

As per **claim 8**, all of the elements of claim 7, from which the claim depends, are discussed in the rejection of claim 6 above, wherein the circuit is pipelined circuit (i.e., part of the pipeline stages) as discussed in the abstract and further the circuit

is further loop-free as describe in section 4.1 (page 18) in which the combinational loops are converted to the equivalent latch or combinational logic, for which the verification applies.

Allowable Subject Matter

8. **Claims 9-24** would be allowable if rewritten to overcome the minor informalities, set forth in this Office action.

9. The following is a statement of reasons for the indication of allowable subject matter:

10. As per **claims 9-24**, the independent claims 9, 20,22, from which the claims depend respectively, recite the method/system/computer readable media comprising the inventive steps/means/code for listing/placing the latches in a predetermined order in combination with the representing and computing steps/means/code as claimed, which corresponds to Applicant's specification, paragraph [14], page 4 to paragraph [51], page 14, (see especially page 11, paragraph [41]), which the prior arts made of record failed to teach or suggest. In particular, the prior arts made of record teach various methods/systems for equivalence verification, including the use of ordering or pre-ordering latches (see especially **Prasad et al.**, U.S. Patent Application Publication No. 2004/0237057, especially paragraphs [0017]-[0018], [0028]-[0029]; **Jain**, U.S. Patent Application Publication No. 2004/0098682, especially paragraphs [0006], [0024], [0101]; **Burch et al.**, U.S. Patent No. 6,247,163, especially col. 2, lines 51-63; col. 5, lines 52-61; col. 9, line 24 to col. 10, line 10; **Bischoff et al.**, "Formal Implementation Verification of the Bus Interface Unit for the Alpha 21264 Microprocessor", Proceedings

of the 1997 IEEE International Conference on Computer Design: VLSI Computers and Processors, 12 October 1997, pp. 16-24, especially Fig. 3). However, the prior arts made of record failed to teach or suggest the combinations of the inventive steps/means as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is herein requested to consider them carefully in response to this Office Action. In particular, the following prior arts made of record are most relevant:

Prasad et al. (U.S. Patent Application Publication No. 2004/0237057, especially paragraphs [0017]-[0018], [0028]-[0029]);

Jain (U.S. Patent Application Publication No. 2004/0098682, especially paragraphs [0006], [0024], [0101]);

Burch et al. (U.S. Patent No. 6,247,163, especially col. 2, lines 51-63; col. 5, lines 52-61; col. 9, line 24 to col. 10, line 10).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Friday, 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
U.S. Patent Examiner
October 1, 2005